

CLMPTO

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CLAIMS 1-39 (CANCELLED)

40. (Previously Presented) A thin film transistor (TFT) array panel, comprising:
a gate wire formed on an insulating substrate;
a gate insulating layer covering the gate wire;
a semiconductor layer formed on the gate insulating layer;
a data wire formed on the gate insulating layer and the semiconductor layer;
a passivation layer covering the data wire; and
a transparent conductive layer formed of indium zinc oxide (IZO),
wherein at least one of the gate wire and the data wire is formed of a conductive layer
containing aluminum, and the transparent conductive layer is connected to and in direct contact
with the conductive layer.

41. (Cancelled)

42. (Previously Presented) The TFT array panel of claim 40, wherein the data wire
has a flat surface.

43. (Previously Presented) The TFT array panel of claim 40, wherein the insulating
layer and the passivation layer are made of silicon-nitride.

44. (Cancelled)

45. (Previously Presented) The TFT array panel of claim 40, wherein the gate wire includes a gate line, a gate electrode connected to the gate line, and a gate pad connected to the gate line, and

the data wire includes a data line, a source electrode connected to the data line, a drain electrode separated from the source electrode and opposite to the source electrode with respect to the gate electrode, and a data pad connected to the data line.

46. (Previously Presented) The TFT array panel of claim 45, wherein the passivation layer further comprises a second contact hole exposing the data pad and a third contact hole exposing the gate pad along with the gate insulating layer, the first to the third contact holes have a shape including rounds or corner, and a size of the first to the third contact holes are greater than $4\ \mu\text{m} * 4\ \mu\text{m}$.

47. (Previously Presented) The TFT array panel of claim 40, wherein the conductive layer is formed of aluminum or an aluminum alloy.

48. (Previously Presented) The TFT array panel of claim 47, wherein the transparent conductive layer comprises:

a first pattern directly contacting and connected to the gate wire through the gate insulating layer; and

a second pattern directly contacting and connected to the data wire through the passivation layer.

49. (Previously Presented) A thin film transistor (TFT) array panel, comprising:
a substrate;
a gate wire formed on the substrate and comprising a gate pad and a gate line extended from the gate pad;
a gate insulating layer covering the gate wire;
a data wire formed on the gate insulating layer and comprising a data line, a source electrode connected to the data line and a drain electrode separated from the source electrode;
a passivation layer covering the data wire; and
a transparent conductive layer formed of indium zinc oxide (IZO),
wherein at least one of the gate pad and the drain electrode is formed of a conductive layer containing aluminum, and the transparent conductive layer is connected to and in direct contact with the conductive layer.

50. (Previously Presented) The TFT array panel of claim 49, wherein the conductive layer is formed of aluminum or an aluminum alloy.

51. (Currently Amended) The TFT array panel of claim 50, wherein the conductive layer is formed of an Al-Nd alloy.

52. (Previously Presented) The TFT array panel of claim 49, wherein the passivation layer is formed of silicon nitride.

53. (Previously Presented) The TFT array panel of claim 49, wherein the transparent conductive layer formed of IZO is formed from an IZO target including In_2O_3 and ZnO with a Zn content ranged between 15% to 20%.

54. (Cancelled)

55. (Previously Presented) The TFT array panel of claim 40, wherein the transparent conductive layer formed of IZO is formed from an IZO target including In_2O_3 and ZnO with a Zn content ranged between 15% to 20%.

56. (Previously Presented) The TFT array panel of claim 47, wherein the conductive layer is formed of an Al-Nd alloy.